CLAIM AMENDMENTS

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) An apparatus comprising:

~~a plurality of processing elements, that process data based on content of the data stored in a plurality of associated memory, to iteratively decode a received codeword using a bit reliability such that for each iteration the bit reliability is updated based on a comparison using a threshold comprising a plurality of threshold values that are updated during the iterative decoding.~~

a plurality of processing elements operating based on associative processing, the plurality of processing elements coupled to perform operations in word-parallel, bit-serial format, wherein the plurality of processing elements are further coupled to iteratively decode a received codeword using a bit reliability value such that for each iteration, the bit reliability value is updated based on a comparison using a threshold value based on a plurality of threshold values that are updated during the iterative decoding, each processing element in the plurality of processing elements further including:

a memory unit for storing data, wherein the data stored within the memory unit is identified based on memory content rather than an address; and

a processing logic unit for comparing the bit reliability value with the threshold value.

2. (Currently Amended) The apparatus of claim 1, wherein the plurality of processing elements ~~comprise~~ includes input processing elements, row control elements, column control elements, and associative processing elements arranged in one or more rows and columns based on a presence of a first logic level present in each row and column of a low-density parity check matrix.

3. (Currently Amended) The apparatus of claim 2, wherein each column further comprises an input processing element that determines an initial bit reliability and an

initial hard decision value for bit positions of a codeword based on soft decision values, wherein the codeword is generated based on the low-density parity check parity matrix and the soft decision values are generated based on a likelihood that a bit represents a first value.

4. (Original) The apparatus of claim 3, wherein the input processing element generate

the initial bit reliability as equaling an absolute value of a value corresponding to the bit positions, and

the initial hard decision value as equaling a second value if the soft decision value is positive and a third value otherwise.

5. (Original) The apparatus of claim 2, wherein a first row of the rows comprises a first set of associative processing elements and a first row control element, which, collectively, determine a first minimum value and a second minimum value of bit reliability values stored in the first set of associative processing elements during a first iteration.

6. (Original) The apparatus of claim 5, wherein the first row control element

stores the first minimum value in the first set of associative processing element comprising a value other than the first minimum value, and

stores the second minimum value in the first set of associative processing elements that stored the first minimum value before the first iteration.

7. (Original) The apparatus of claim 5, wherein the first row control element

generates one or more control values comprising a first comparand and a mask to determine the presence of the first minimum value in the first set of associative processing element, a second comparand and a mask to determine the presence of the second minimum value in the first set of associative processing element,

receives one or more decision values indicating presence of one or more of the first minimum value and the second minimum value, and

determines the first minimum value and the second minimum value based on the one or more decision values.

8. (Currently Amended) The apparatus of claim 7, wherein the first set of associative processing elements

receives the one or more control values, and

generates the one or more decision values comprising a first value indicating a presence of the first minimum value in at least one of the first associative processing elements, a second value indicating a presence of the second minimum value in at least one of the first associative processing elements, and a third value indicating a presence of the first minimum value in at least two of the first associative processing elements.

9. (Currently Amended) The apparatus of claim 8, the first set of associative processing elements comprise a first element, which further comprises

[[a]] logic inside the processing logic unit to receive the one or more control values and generate update values, wherein the update values represent a result of comparison of masked on bits of the first comparand and the bit reliability value stored in the first element, and

a set of logic gates inside the processing logic unit to generate the one or more decision values based on the update values and send the decision values to a second element.

10. (Original) The apparatus of claim 2, wherein a first column of the columns comprise a first input processing element, a first column control element, and a second set of the associative processing elements, which, collectively, determine a first bit of an updated hard decision vector.

11. (Original) The apparatus of claim 10, wherein the first input processing element, the first column control element, and the second set of the associative processing elements, collectively, determine a first bit of an updated hard decision vector based on a first comparison reliability value and a first threshold value of the plurality of threshold

values.

12. (Original) The apparatus of claim 11, wherein the first input processing element, the first column control element, and the second set of the associative processing elements, collectively, determine the first comparison reliability value based on a first check sum determined based on the hard decision values and a first minimum value representing a minimum value of the bit reliability stored in a first set of associative processing elements of a first row.

13. (Currently Amended) The apparatus of claim 1, wherein the plurality of processing elements determine the plurality of threshold values based on a first characteristic of a communication channel over which a [[the]] low-density parity check codeword is received.

14. (Currently Amended) The apparatus of claim 1, wherein the plurality of processing elements continue to iteratively decode a [[the]] low-density parity check codeword until a desired data stream is generated.

15. (Currently Amended) The apparatus of claim 1, wherein the plurality of processing elements continue to iteratively decode a [[the]] low-density parity check codeword for log2 n number of iterations, where n is a code length of the codeword.

16. (Original) A method comprising determining a first minimum value and a second minimum value of bit reliability values stored in a first set of associative processing elements during a first iteration.

17. (Original) The method of claim 16 further comprises

storing the first minimum value in the first set of associative processing element comprising a value other than the first minimum value, and

storing the second minimum value in the first set of associative processing elements that stored the first minimum value before the first iteration.

18. (Original) The method of claim 16 further comprises

generating one or more control values comprising a first comparand and a mask to determine the presence of the first minimum value in the first set of associative processing element,

generating a second comparand and a mask to determine the presence of the second minimum value in the first set of associative processing element,

receiving one or more decision values indicating presence of one or more of the first minimum value and the second minimum value, and

determining the first minimum value and the second minimum value based on the one or more decision values.

19. (Original) The method of claim 18 further comprises

receiving the one or more control values,

generating the one or more decision values comprising a first value indicating a presence of the first minimum value in at least one of the first associative processing elements,

generating the one or more decision values comprising a second value indicating a presence of the second minimum value in at least one of the first associative processing elements, and

generating the one or more decision values comprising a third value indicating a presence of the first minimum value in at least two of the first associative processing elements.

20. (Original) The method of claim 19 further comprises

receiving the one or more control values,

generating a first update value, wherein the first update value represents a result of comparison of masked-in bits of the first comparand and a first bit reliability value, and

generating a second update value, wherein the second update value represents a result of comparison of masked-in bits of the second comparand and a first bit reliability

value.

21. (Currently Amended) A system comprising:

a transmitter;[[,]]

a network interface to receive one or more codewords over a communication medium;[[,]]

a receiver comprising a demodulator to generate soft decisions for the one or more codewords based on one or more characteristics of the communication medium; and

a decoder comprising:

a plurality of processing elements operating based on associative processing, the plurality of processing elements coupled to perform operations in word-parallel, bit-serial format, wherein the plurality of processing elements are further coupled to iteratively decode a received codeword using a bit reliability value such that for each iteration, the bit reliability value is updated based on a comparison using a threshold value based on a plurality of threshold values that are updated during the iterative decoding, each processing element in the plurality of processing elements further including:

a memory unit for storing data, wherein the data stored within the memory unit is identified based on memory content rather than an address; and

a processing logic unit for comparing the bit reliability value with the threshold value.

~~a plurality of processing elements, processing data based on content of the data stored in a plurality of associated memory, to iteratively decode a first codeword of the one or more codewords using a bit reliability such that for each iteration the bit reliability is updated based on a comparison using a threshold comprising a plurality of threshold values that are updated during the iterative decoding.~~

22. (Original) The system of claim 21 wherein the receiver receives the one or more codewords at a rate of at least 10 giga bits per second in accordance with 10GBase-T standard.

23. (Currently Amended) The system of claim 21 further comprises

generating the one or more codewords by encoding a bit stream based on a low-density parity check codes and sending the one or more codewords over the communication medium, and the network interface to transmit the one or more codewords at a rate of at least 10 giga bits over the communication medium.

24. (Original) The system of claim 21 represents a network interface card.

25. (Original) The system of claim 21 the system further includes at least one of a computer, a switch, a router, a handheld, a cell phone, or a server.

26. (New) The method of claim 16, wherein the first set of associative processing elements:

determines the first minimum value and the second minimum value of bit reliability values by identifying the content of the first and second minimum values rather than identifying the address of the first and second minimum values contained in an on-board memory; and

performs operations in word-parallel, bit-serial format.